Digital Design Lab 8

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**Abstract**

The purpose of this lab was to write VHDL code for a rising-edge triggered T flip flop with an asynchronous active low reset. The code was written in Quartus II. The code was compiled and tested using a simulation.

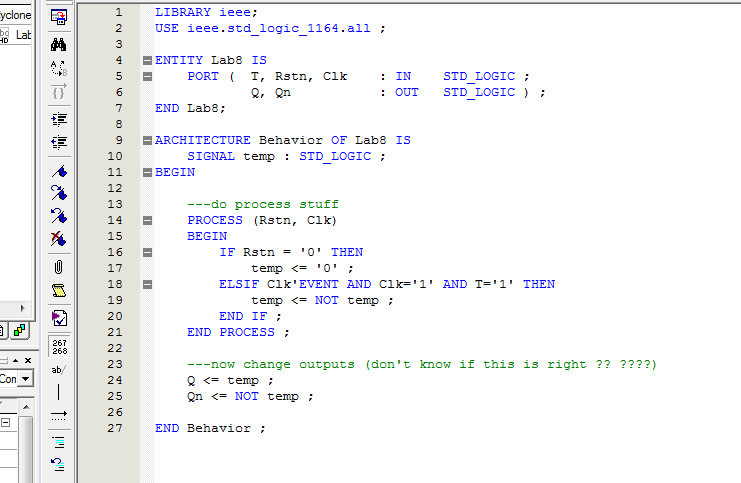
**Introduction**

A T flip-flop takes in three inputs: Clk, a clock input; T, a 1-bit toggle input; and Rstn, a 1-bit asynchronous active-low input. When T is set to 1, Q and Qn are inverted and outputted. When T is set to 0, Q and Qn are outputted without being inverted. The active-low input was designed to set Q and Qn to 0 and 1 when the input was low.

In this lab, the user created a T flip flop by writing VHDL code in Quartus II. The circuit was created and simulated in Quartus II. The circuit was tested using a waveform file. The flip flop compiled and outputted the expected results when tested.

**Design and Implementation**

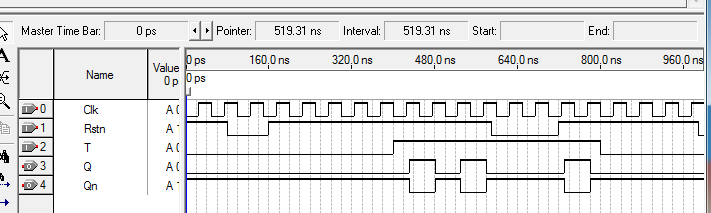
In order to write VHDL code for a T flip flop, a new project was created in Quartus II. A VHDL file was added to it, and code was written to implement the T flip flop. The code is shown in Figure 1 below.



**Figure 1**: VHDL code for T flip flop with asynchronous active-low reset.

The variable 'temp' was an internal signal used to change the outputs Q and Qn when T equaled 1. An internal signal was used because the outputs Q and Qn could not be assigned to other outputs.

The code was compiled, and a waveform file was created to test it. The results of the simulation are shown in Figure 2 below.



**Figure 2**: simulation results for T flip flop with asynchronous active-low reset.

The simulation showed that the T flip flop did everything it was supposed to. Whenever Rstn equaled 0, Q was set to 0 almost immediately (ignoring the gate delay). When T equaled 0, Q and Qn didn't change at all. When T and Rstn equaled 1, Q and Qn changed their outputs as soon as the next rising edge of the clock came, ignoring delay.

**Results**

The circuit correctly toggled Q when T equaled 1 and held Q's value when T equaled 0.

**Conclusion**

The lab was designed to give students a hands-on experience with writing VHDL code to implement a T flip flop with an asynchronous active low input. Using Quartus II, code for a T flip flop was written and tested with a simulation. The lab took about 30 minutes to complete.